Pin List: ZEM4310

2025-07-03

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	0	DGND	DGND		0								JP2A/B/C	2,39
J2	1	XCVR_TXp7			1									
J2	2	XCVR_RXp7			2									
J2	3	XCVR_TXn7			3									
J2	4	XCVR_RXn7			4									
J2	5		+VDC	5									JP2A	3,5
J2	6		+VDC	6									JP2A	3,5
J2	7	XCVR_TXp6			5									
J2	8	XCVR_RXp6			6									
J2	9	XCVR_TXn6			7									
J2	10	XCVR_RXn6			8									
J2	11		+VDC	11									JP2A	3,5
J2	12		+VDC	12									JP2A	3,5
J2	13	XCVR_TXp5			9									
J2	14	XCVR_RXp5			10									
J2	15	XCVR_TXn5			11									
J2	16	XCVR_RXn5			12									
J2	17		+VCCIO4	17									JP2A	7
J2	18		+Y_HSMC_VCCIO	18									JP2A/B/C	40
J2	19	XCVR_TXp4			13									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	20	XCVR_RXp4			14									
J2	21	XCVR_TXn4			15									
J2	22	XCVR_RXn4			16									
J2	23		+VCCIO5	23									JP2A	9
J2	24		Y_HSMC_VS0	24									JP2A	10
J2	25	XCVR_TXp3			17									
J2	26	XCVR_RXp3			18									
J2	27	XCVR_TXn3			19									
J2	28	XCVR_RXn3			20									
J2	29		+VCCIO6	29									JP2A	11
J2	30		Y_HSMC_VS1	30									JP2A	12
J2	31	XCVR_TXp2			21									
J2	32	XCVR_RXp2			22									
J2	33	XCVR_TXn2			23									
J2	34	XCVR_RXn2			24									
J2	35		VREF_BANK4	35									JP2A	13
J2	36		Y_HSMC_VS2	36									JP2A	14
J2	37	XCVR_TXp1			25									
J2	38	XCVR_RXp1			26									
J2	39	XCVR_TXn1			27									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	40	XCVR_RXn1			28									
J2	41		VREF_BANK5	41									JP2A	15
J2	42		VREF_BANK6	42									JP2A	16
J2	43	XCVR_TXp0	PLL4_CLKOUTp	43	29	T16	IO, PLL4_CLKOUTp	4	24.137				JP2A	19
J2	44	XCVR_RXp0			30									
J2	45	XCVR_TXn0	PLL4_CLKOUTn	45	31	R16	IO, PLL4_CLKOUTp	4	23.764				JP2A	21
J2	46	XCVR_RXn0			32									
J2	47													
J2	48		+2.5VDD	48									JP2A	18
J2	49	SDA	HSMC_SDA		33	Y4	B3p	3					JP2A	23
J2	50	SCL	HSMC_SCL		34	AA4	IO	3					JP2A	20
J2	51	JTAG_TCK	JTAG_TCK		35								JP2A	25
J2	52	JTAG_TMS	JTAG_TMC		36								JP2A	22
J2	53													
J2	54													
J2	55	JTAG_TDO	JTAG_TDO		37								JP2A	27
J2	56	JTAG_TDI	JTAG_TDI		38								JP2A	24
J2	57	CLKOUT0	CLKOUT0		39	V13	B31p	4	54.058				JP2A	29
J2	58	CLKIN0	CLKIN0		40	T22	CLK7,DIFFCLK_3n	5	53.848				JP2A	26
J2	59		CHARGE_DETECT	59									JP2A	17

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	60													
J2	61	D0	D0		41	U12	B28p	4	53.848				JP2A	31
J2	62	D1	D1		42	U13	B32p	4	54.019				JP2A	28
J2	63	D2	D2		43	W15	B35p	4	53.848				JP2A	33
J2	64	D3	D3		44	AB18	IO	4	53.952				JP2A	30
J2	65	+3.3VDD	+3.3VDD		45								JP2A/B/C	1
J2	66	+12VDD	+12VDD		46									
J2	67	D4 / LVDS_TXp0	D4 / LVDS_TXp0		47	J19	R10p	6	54.241				JP2A	35
J2	68	D5 / LVDS_RXp0	D5 / LVDS_RXp0		48	AA13	B23p	4	54.221	R71			JP2A	32
J2	69	D6 / LVDS_TXn0	D6 / LVDS_TXn0		49	J20	R10n	6	54.233				JP2A	37
J2	70	D7 / LVDS_RXn0	D7 / LVDS_RXn0		50	AB13	B23n	4	54.108	R71			JP2A	34
J2	71	+3.3VDD	+3.3VDD		51									
J2	72	+12VDD	+12VDD		52									
J2	73	D8 / LVDS_TXp1	D8 / LVDS_TXp1		53	H17	R5p	6	53.784				JP2B	3
J2	74	D9 / LVDS_RXp1	D9 / LVDS_RXp1		54	AA14	B25p	4	54.290	R72			JP2B	4
J2	75	D10 / LVDS_TXn1	D10 / LVDS_TXn1		55	G18	R5n	6	53.876				JP2B	5
J2	76	D11 / LVDS_RXn1	D11 / LVDS_RXn1		56	AB14	B25n	4	54.249	R72			JP2B	6
J2	77	+3.3VDD	+3.3VDD		57									
J2	78	+12VDD	+12VDD		58									
J2	79	D12 / LVDS_TXp2	D12 / LVDS_TXp2		59	K18	R13p	6	53.983				JP2B	7

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	80	D13 / LVDS_RXp2	D13 / LVDS_RXp2		60	W13	B26p	4	53.544	R73			JP2B	8
J2	81	D14 / LVDS_TXn2	D14 / LVDS_TXn2		61	K17	R13n	6	54.080				JP2B	9
J2	82	D15 / LVDS_RXn2	D15 / LVDS_RXn2		62	Y13	B26n	4	53.573	R73			JP2B	10
J2	83	+3.3VDD	+3.3VDD		63									
J2	84	+12VDD	+12VDD		64									
J2	85	D16 / LVDS_TXp3	D16 / LVDS_TXp3		65	M19	R18p	5	53.623				JP2B	11
J2	86	D17 / LVDS_RXp3	D17 / LVDS_RXp3		66	AA15	B27p	4	54.097	R74			JP2B	12
J2	87	D18 / LVDS_TXn3	D18 / LVDS_TXn3		67	M20	R18n	5	53.725				JP2B	13
J2	88	D19 / LVDS_RXn3	D19 / LVDS_RXn3		68	AB15	B27n	4	54.036	R74			JP2B	14
J2	89	+3.3VDD	+3.3VDD		69									
J2	90	+12VDD	+12VDD		70									
J2	91	D20 / LVDS_TXp4	D20 / LVDS_TXp4		71	N21	R20p	5	53.797				JP2B	15
J2	92	D21 / LVDS_RXp4	D21 / LVDS_RXp4		72	AA16	B30p	4	53.713	R75			JP2B	16
J2	93	D22 / LVDS_TXn4	D22 / LVDS_TXn4		73	N22	R20n	5	53.848				JP2B	17
J2	94	D23 / LVDS_RXn4	D23 / LVDS_RXn4		74	AB16	B30n	4	53.785	R75			JP2B	18
J2	95	+3.3VDD	+3.3VDD		75									
J2	96	+12VDD	+12VDD		76									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	97	D24 / LVDS_TXp5	D24 / LVDS_TXp5		77	H19	R9p	6	53.669				JP2B	19
J2	98	D25 / LVDS_RXp5	D25 / LVDS_RXp5		78	AA17	B37p	4	54.098	R76			JP2B	20
J2	99	D26 / LVDS_TXn5	D26 / LVDS_TXn5		79	H20	R9n	6	53.652				JP2B	21
J2	100	D27 / LVDS_RXn5	D27 / LVDS_RXn5		80	AB17	B37n	4	54.000	R76			JP2B	22
J2	101	+3.3VDD	+3.3VDD		81									
J2	102	+12VDD	+12VDD		82									
J2	103	D28 / LVDS_TXp6	D28 / LVDS_TXp6		83	M21	R19p	5	53.716				JP2B	23
J2	104	D29 / LVDS_RXp6	D29 / LVDS_RXp6		84	AA20	B39p	4	53.782	R77			JP2B	24
J2	105	D30 / LVDS_TXn6	D30 / LVDS_TXn6		85	M22	R19n	5	53.720				JP2B	25
J2	106	D31 / LVDS_RXn6	D31 / LVDS_RXn6		86	AB20	B39n	4	53.844	R77			JP2B	26
J2	107	+3.3VDD	+3.3VDD		87									
J2	108	+12VDD	+12VDD		88									
J2	109	D32 / LVDS_TXp7	D32 / LVDS_TXp7		89	J21	R15p	6	53.991				JP2B	27
J2	110	D33 / LVDS_RXp7	D33 / LVDS_RXp7		90	Y14	B29p	4	54.059	R78			JP2B	28
J2	111	D34 / LVDS_TXn7	D34 / LVDS_TXn7		91	J22	R15n	6	53.948				JP2B	29

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	112	D35 / LVDS_RXn7	D35 / LVDS_RXn7		92	Y15	B29n	4	53.987	R78			JP2B	30
J2	113	+3.3VDD	+3.3VDD		93									
J2	114	+12VDD	+12VDD		94									
J2	115	D36 / CLKOUT1p	D36 / CLKOUT1p		95	R21	R24p	5	53.599				JP2B	31
J2	116	D37 / CLKIN1p	D37 / CLKIN1p		96	L21	R17p	6	53.848 / 53.125	R88	See UM for CLKIN jumper selection. Move R103 to R101 for FPGA pin G21 (CLK4, DIFFCLK_2p) in Bank 6.		JP2B	32
J2	117	D38 / CLKOUT1n	D38 / CLKOUT1n		97	R22	R24n	5	53.705				JP2B	33
J2	118	D39 / CLKIN1n	D39 / CLKIN1n		98	L22	R17n	6	53.848 / 53.158	R88	See UM for CLKIN jumper selection. Move R105 to R107 for FPGA pin G22 (CLK5, DIFFCLK_2n) in Bank 6.		JP2B	34
J2	119	+3.3VDD	+3.3VDD		99									
J2	120	+12VDD	+12VDD		100									
J2	121	D40 / LVDS_TXp8	D40 / LVDS_TXp8		101	F21	R11p	6	53.920				JP2B	35
J2	122	D41 / LVDS_RXp8	D41 / LVDS_RXp8		102	V14	B33p	4	53.835	R79			JP2B	36
J2	123	D42 / LVDS_TXn8	D42 / LVDS_TXn8		103	F22	R11n	6	53.848				JP2B	37
J2	124	D43 / LVDS_RXn8	D43 / LVDS_RXn8		104	U14	B33n	4	53.868	R79			JP2B	38
J2	125	+3.3VDD	+3.3VDD		105									
J2	126	+12VDD	+12VDD		106									
J2	127	D44 / LVDS_TXp9	D44 / LVDS_TXp9		107	H21	R14p	6	53.667				JP2C	3

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	128	D45 / LVDS_RXp9	D45 / LVDS_RXp9		108	W17	B38p	4	54.377	R80			JP2C	4
J2	129	D46 / LVDS_TXn9	D46 / LVDS_TXn9		109	H22	R14n	6	53.702				JP2C	5
J2	130	D47 / LVDS_RXn9	D47 / LVDS_RXn9		110	Y17	B38n	4	54.381	R80			JP2C	6
J2	131	+3.3VDD	+3.3VDD		111									
J2	132	+12VDD	+12VDD		112									
J2	133	D48 / LVDS_TXp10	D48 / LVDS_TXp10		113	E21	R8p	6	53.638				JP2C	7
J2	134	D49 / LVDS_RXp10	D49 / LVDS_RXp10		114	P21	R23p	5	53.594	R81			JP2C	8
J2	135	D50 / LVDS_TXn10	D50 / LVDS_TXn10		115	E22	R8n	6	53.643				JP2C	9
J2	136	D51 / LVDS_RXn10	D51 / LVDS_RXn10		116	P22	R23n	5	53.674	R81			JP2C	10
J2	137	+3.3VDD	+3.3VDD		117									
J2	138	+12VDD	+12VDD		118									
J2	139	D52 / LVDS_TXp11	D52 / LVDS_TXp11		119	F19	R6p	6	53.580				JP2C	11
J2	140	D53 / LVDS_RXp11	D53 / LVDS_RXp11		120	U16	B40p	4	53.885	R82			JP2C	12
J2	141	D54 / LVDS_TXn11	D54 / LVDS_TXn11		121	F20	R6n	6	53.561				JP2C	13
J2	142	D55 / LVDS_RXn11	D55 / LVDS_RXn11		122	U17	B40n	4	53.817	R82			JP2C	14

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	143	+3.3VDD	+3.3VDD		123									
J2	144	+12VDD	+12VDD		124									
J2	145	D56 / LVDS_TXp12	D56 / LVDS_TXp12		125	D21	R7p	6	53.803				JP2C	15
J2	146	D57 / LVDS_RXp12	D57 / LVDS_RXp12		126	T14	B36p	4	54.310	R83			JP2C	16
J2	147	D58 / LVDS_TXn12	D58 / LVDS_TXn12		127	D22	R7n	6	53.848				JP2C	17
J2	148	D59 / LVDS_RXn12	D59 / LVDS_RXn12		128	T15	B36n	4	54.221	R83			JP2C	18
J2	149	+3.3VDD	+3.3VDD		129									
J2	150	+12VDD	+12VDD		130									
J2	151	D60 / LVDS_TXp13	D60 / LVDS_TXp13		131	C21	R4p	6	54.098				JP2C	19
J2	152	D61 / LVDS_RXp13	D61 / LVDS_RXp13		132	N19	R22p	5	54.131	R84			JP2C	20
J2	153	D62 / LVDS_TXn13	D62 / LVDS_TXn13		133	C22	R4n	6	54.009				JP2C	21
J2	154	D63 / LVDS_RXn13	D63 / LVDS_RXn13		134	N20	R22n	5	54.044	R84			JP2C	22
J2	155	+3.3VDD	+3.3VDD		135									
J2	156	+12VDD	+12VDD		136									
J2	157	D64 / LVDS_TXp14	D64 / LVDS_TXp14		137	B21	R3p	6	53.866				JP2C	23
J2	158	D65 / LVDS_RXp14	D65 / LVDS_RXp14		138	N18	R21p	5	54.014	R85			JP2C	24

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	159	D66 / LVDS_TXn14	D66 / LVDS_TXn14		139	B22	R3n	6	53.848				JP2C	25
J2	160	D67 / LVDS_RXn14	D67 / LVDS_RXn14		140	N17	R21n	5	54.038	R85			JP2C	26
J2	161	+3.3VDD	+3.3VDD		141									
J2	162	+12VDD	+12VDD		142									
J2	163	D68 / LVDS_TXp15	D68 / LVDS_TXp15		143	D20	R2p	6	53.549				JP2C	27
J2	164	D69 / LVDS_RXp15	D69 / LVDS_RXp15		144	R14	B41p	4	54.188	R86			JP2C	28
J2	165	D70 / LVDS_TXn15	D70 / LVDS_TXn15		145	C20	R2n	6	53.456				JP2C	29
J2	166	D71 / LVDS_RXn15	D71 / LVDS_RXn15		146	R15	B41n	4	54.105	R86			JP2C	30
J2	167	+3.3VDD	+3.3VDD		147									
J2	168	+12VDD	+12VDD		148									
J2	169	D72 / LVDS_TXp16	D72 / LVDS_TXp16		149	G17	R1p	6	53.436				JP2C	31
J2	170	D73 / LVDS_RXp16	D73 / LVDS_RXp16		150	U15	B34p	4	54.291	R87			JP2C	32
J2	171	D74 / LVDS_TXn16	D74 / LVDS_TXn16		151	F17	R1n	6	53.476				JP2C	33
J2	172	D75 / LVDS_RXn16	D75 / LVDS_RXn16		152	V15	B34n	4	54.266	R87			JP2C	34
J2	173	+3.3VDD	+3.3VDD		153									
J2	174	+12VDD	+12VDD		154									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J2	175	D76 / CLKOUT2p	D76 / CLKOUT2p		155	K21	R16p	6	54.032				JP2C	35
J2	176	D77 / CLKIN2p	D77 / CLKIN2p		156	J18	R12n	6	54.298 / 53.903	R89	See UM for CLKIN jumper selection. Move R111 to R109 for FPGA pin AA12 (CLK13, DIFFCLK_7p) in Bank 4. See PCB revision notes in UM.		JP2C	36
J2	177	D78 / CLKOUT2n	D78 / CLKOUT2n		157	K22	R16n	6	53.973				JP2C	37
J2	178	D79 / CLKIN2n	D79 / CLKIN2n		158	J17	IO	6	53.848 / 53.806	R89	See UM for CLKIN jumper selection. Move R113 to R115 for FPGA pin AB12 (CLK12, DIFFCLK_7n) in Bank 4. See PCB revision notes in UM.		JP2C	38
J2	179	+3.3VDD	+3.3VDD		159									
J2	180	PRSNTn	PRSNTn		160						Present Detect			
J1	0	DGND	DGND		0								JP1A/B/C	2,39
J1	1	XCVR_TXp7			1									
J1	2	XCVR_RXp7			2									
J1	3	XCVR_TXn7			3									
J1	4	XCVR_RXn7			4									
J1	5		+VCCIO2	5									JP1A	3
J1	6		+1.2VDD	6									JP1A	4
J1	7	XCVR_TXp6			5									
J1	8	XCVR_RXp6			6									
J1	9	XCVR_TXn6			7									
J1	10	XCVR_RXn6			8									
J1	11		+VCCIO3	11									JP1A	5
J1	12		+1.8VDD	12									JP1A	6
J1	13	XCVR_TXp5			9									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	14	XCVR_RXp5			10									
J1	15	XCVR_TXn5			11									
J1	16	XCVR_RXn5			12									
J1	17		VREF_BANK2	17									JP1A	7
J1	18		+X_HSMC_VCCIO	18									JP1A/B/C	40
J1	19	XCVR_TXp4			13									
J1	20	XCVR_RXp4			14									
J1	21	XCVR_TXn4			15									
J1	22	XCVR_RXn4			16									
J1	23		VREF_BANK3	23									JP1A	9
J1	24		X_HSMC_VS0	24									JP1A	10
J1	25	XCVR_TXp3			17									
J1	26	XCVR_RXp3			18									
J1	27	XCVR_TXn3			19									
J1	28	XCVR_RXn3			20									
J1	29		BANK1_CLK	29		G1	CLK1, DIFFCLK_0n	1	24.701				JP1A	11
J1	30		X_HSMC_VS1	30									JP1A	12
J1	31	XCVR_TXp2			21									
J1	32	XCVR_RXp2			22									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	33	XCVR_TXn2			23									
J1	34	XCVR_RXn2			24									
J1	35		BANK8_CLK	35		B11	CLK11, DIFFCLK_4p	8	53.554				JP1A	13
J1	36		X_HSMC_VS2	36									JP1A	14
J1	37	XCVR_TXp1			25									
J1	38	XCVR_RXp1			26									
J1	39	XCVR_TXn1			27									
J1	40	XCVR_RXn1			28									
J1	41													
J1	42		JP3_JTAG_TDI	42									JP8	9
J1	43	XCVR_TXp0	PLL1_CLKOUTp	43	29	AA3	IO, PLL1_CLKOUTp	3	46.897				JP1A	19
J1	44	XCVR_RXp0			30									
J1	45	XCVR_TXn0	PLL1_CLKOUTn	45	31	AB3	IO, PLL1_CLKOUTn	3	45.867				JP1A	21
J1	46	XCVR_RXn0			32									
J1	47													
J1	48		JP3_JTAG_TDO	48									JP8	3
J1	49	SDA	HSMC_SDA		33	W8	IO	3					JP1A	23
J1	50	SCL	HSMC_SCL		34	U10	B16n	3					JP1A	20
J1	51	JTAG_TCK	JTAG_TCK		35								JP1A	25

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	52	JTAG_TMS	JTAG_TMC		36								JP1A	22
J1	53													
J1	54		JP3_JTAG_TMS	54									JP8	5
J1	55	JTAG_TDO	JTAG_TDO		37								JP1A	27
J1	56	JTAG_TDI	JTAG_TDI		38								JP1A	24
J1	57	CLKOUT0	CLKOUT0		39	V10	B15p	3	64.062				JP1A	29
J1	58	CLKIN0	CLKIN0		40	T21	CLK6, DIFFCLK_3p	5	64.404			pix_clk	JP1A	26
J1	59		OVP_FLAG	59									JP1A	17
J1	60		JP3_JTAG_TCK	60									JP8	1
J1	61	D0	D0		41	U9	B8p	3	64.389			pix_extclk	JP1A	31
J1	62	D1	D1		42	V8	B8n	3	64.455			pix_reset	JP1A	28
J1	63	D2	D2		43	Y3	B3n	3	64.389			pix_data[0]	JP1A	33
J1	64	D3	D3		44	Y6	IO	3	64.761			pix_trigger	JP1A	30
J1	65	+3.3VDD	+3.3VDD		45								JP1A/B/C	1
J1	66	+12VDD	+12VDD		46									
J1	67	D4 / LVDS_TXp0	D4 / LVDS_TXp0		47	L6	L16p	2	64.044			pix_data[1]	JP1A	35
J1	68	D5 / LVDS_RXp0	D5 / LVDS_RXp0		48	V6	B1p	3	64.976	R23		pix_strobe	JP1A	32
J1	69	D6 / LVDS_TXn0	D6 / LVDS_TXn0		49	M6	L16n	2	64.049			pix_data[2]	JP1A	37
J1	70	D7 / LVDS_RXn0	D7 / LVDS_RXn0		50	V5	B1n	3	64.964	R23		pix_data[9]	JP1A	34

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	71	+3.3VDD	+3.3VDD		51									
J1	72	+12VDD	+12VDD		52									
J1	73	D8 / LVDS_TXp1	D8 / LVDS_TXp1		53	M2	L17p	2	64.511			pix_data[3]	JP1B	3
J1	74	D9 / LVDS_RXp1	D9 / LVDS_RXp1		54	U7	B2p	3	64.520	R49		pix_data[10]	JP1B	4
J1	75	D10 / LVDS_TXn1	D10 / LVDS_TXn1		55	M1	L17n	2	64.577			pix_data[4]	JP1B	5
J1	76	D11 / LVDS_RXn1	D11 / LVDS_RXn1		56	U8	B2n	3	64.587	R49		pix_data[11]	JP1B	6
J1	77	+3.3VDD	+3.3VDD		57									
J1	78	+12VDD	+12VDD		58									
J1	79	D12 / LVDS_TXp2	D12 / LVDS_TXp2		59	M4	L18p	2	63.994			pix_data[5]	JP1B	7
J1	80	D13 / LVDS_RXp2	D13 / LVDS_RXp2		60	W6	B4p	3	64.093	R54		pix_sclk	JP1B	8
J1	81	D14 / LVDS_TXn2	D14 / LVDS_TXn2		61	M3	L18n	2	64.103			pix_data[6]	JP1B	9
J1	82	D15 / LVDS_RXn2	D15 / LVDS_RXn2		62	V7	B4n	3	63.133	R54		pix_sdata	JP1B	10
J1	83	+3.3VDD	+3.3VDD		63									
J1	84	+12VDD	+12VDD		64									
J1	85	D16 / LVDS_TXp3	D16 / LVDS_TXp3		65	N2	L19p	2	64.365			pix_data[7]	JP1B	11
J1	86	D17 / LVDS_RXp3	D17 / LVDS_RXp3		66	AA5	B5p	3	64.203	R55		pix_fv	JP1B	12
J1	87	D18 / LVDS_TXn3	D18 / LVDS_TXn3		67	N1	L19n	2	64.393			pix_data[8]	JP1B	13

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	88	D19 / LVDS_RXn3	D19 / LVDS_RXn3		68	AA6	B5n	3	64.227	R55		pix_lv	JP1B	14
J1	89	+3.3VDD	+3.3VDD		69									
J1	90	+12VDD	+12VDD		70									
J1	91	D20 / LVDS_TXp4	D20 / LVDS_TXp4		71	P2	L20p	2	64.814				JP1B	15
J1	92	D21 / LVDS_RXp4	D21 / LVDS_RXp4		72	AB6	B6p	3	64.836	R56			JP1B	16
J1	93	D22 / LVDS_TXn4	D22 / LVDS_TXn4		73	P1	L20n	2	64.843				JP1B	17
J1	94	D23 / LVDS_RXn4	D23 / LVDS_RXn4		74	AB5	B6n	3	64.766	R56			JP1B	18
J1	95	+3.3VDD	+3.3VDD		75									
J1	96	+12VDD	+12VDD		76									
J1	97	D24 / LVDS_TXp5	D24 / LVDS_TXp5		77	R2	L21p	2	64.457				JP1B	19
J1	98	D25 / LVDS_RXp5	D25 / LVDS_RXp5		78	W7	B7p	3	64.677	R57		focus_scl	JP1B	20
J1	99	D26 / LVDS_TXn5	D26 / LVDS_TXn5		79	R1	L21n	2	64.474				JP1B	21
J1	100	D27 / LVDS_RXn5	D27 / LVDS_RXn5		80	Y7	B7n	3	64.683	R57		focus_sda	JP1B	22
J1	101	+3.3VDD	+3.3VDD		81									
J1	102	+12VDD	+12VDD		82									
J1	103	D28 / LVDS_TXp6	D28 / LVDS_TXp6		83	P4	L23p	2	64.426				JP1B	23
J1	104	D29 / LVDS_RXp6	D29 / LVDS_RXp6		84	AA7	B10p	3	64.606	R58		focus_sdi	JP1B	24

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	105	D30 / LVDS_TXn6	D30 / LVDS_TXn6		85	P3	L23n	2	64.389				JP1B	25
J1	106	D31 / LVDS_RXn6	D31 / LVDS_RXn6		86	AB7	B10n	3	64.521	R58		focus_sdo	JP1B	26
J1	107	+3.3VDD	+3.3VDD		87									
J1	108	+12VDD	+12VDD		88									
J1	109	D32 / LVDS_TXp7	D32 / LVDS_TXp7		89	U2	L24p	2	64.306				JP1B	27
J1	110	D33 / LVDS_RXp7	D33 / LVDS_RXp7		90	AA8	B17p	3	64.596	R59		focus_sck	JP1B	28
J1	111	D34 / LVDS_TXn7	D34 / LVDS_TXn7		91	U1	L24n	2	64.278				JP1B	29
J1	112	D35 / LVDS_RXn7	D35 / LVDS_RXn7		92	AB8	B17n	3	64.685	R59		focus_ss	JP1B	30
J1	113	+3.3VDD	+3.3VDD		93									
J1	114	+12VDD	+12VDD		94									
J1	115	D36 / CLKOUT1p	D36 / CLKOUT1p		95	R19	R26p	5	64.861				JP1B	31
J1	116	D37 / CLKIN1p	D37 / CLKIN1p		96	AA1	L31n	2	64.389 / 65.097	R69	See UM for CLKIN jumper selection. Move R104 to R102 for FPGA pin AA11 (CLK15, DIFFCLK_6p) in Bank 3. See PCB revision notes in UM.	focus_rst_n	JP1B	32
J1	117	D38 / CLKOUT1n	D38 / CLKOUT1n		97	R18	R26n	5	64.867				JP1B	33
J1	118	D39 / CLKIN1n	D39 / CLKIN1n		98	Y8	B11p	3	64.389 / 65.075	R69	See UM for CLKIN jumper selection. Move R106 to R108 for FPGA pin AB11 (CLK14, DIFFCLK_6n) in Bank 3. See PCB revision notes in UM.		JP1B	34
J1	119	+3.3VDD	+3.3VDD		99									
J1	120	+12VDD	+12VDD		100									

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	121	D40 / LVDS_TXp8	D40 / LVDS_TXp8		101	V2	L25p	2	64.646				JP1B	35
J1	122	D41 / LVDS_RXp8	D41 / LVDS_RXp8		102	T10	B13p	3	64.643	R60			JP1B	36
J1	123	D42 / LVDS_TXn8	D42 / LVDS_TXn8		103	V1	L25n	2	64.645				JP1B	37
J1	124	D43 / LVDS_RXn8	D43 / LVDS_RXn8		104	T11	B13n	3	64.615	R60			JP1B	38
J1	125	+3.3VDD	+3.3VDD		105									
J1	126	+12VDD	+12VDD		106									
J1	127	D44 / LVDS_TXp9	D44 / LVDS_TXp9		107	R4	L27p	2	64.319				JP1C	3
J1	128	D45 / LVDS_RXp9	D45 / LVDS_RXp9		108	AA9	B18p	3	64.454	R61			JP1C	4
J1	129	D46 / LVDS_TXn9	D46 / LVDS_TXn9		109	R3	L27n	2	64.389				JP1C	5
J1	130	D47 / LVDS_RXn9	D47 / LVDS_RXn9		110	AB9	B19n	3	64.389	R61			JP1C	6
J1	131	+3.3VDD	+3.3VDD		111									
J1	132	+12VDD	+12VDD		112									
J1	133	D48 / LVDS_TXp10	D48 / LVDS_TXp10		113	W2	L28p	2	64.302				JP1C	7
J1	134	D49 / LVDS_RXp10	D49 / LVDS_RXp10		114	W10	B20p	3	64.4486	R62			JP1C	8
J1	135	D50 / LVDS_TXn10	D50 / LVDS_TXn10		115	W1	L28n	2	64.257				JP1C	9

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	136	D51 / LVDS_RXn10	D51 / LVDS_RXn10		116	Y10	B20n	3	64.389	R62			JP1C	10
J1	137	+3.3VDD	+3.3VDD		117									
J1	138	+12VDD	+12VDD		118									
J1	139	D52 / LVDS_TXp11	D52 / LVDS_TXp11		119	Y2	L29p	2	65.244				JP1C	11
J1	140	D53 / LVDS_RXp11	D53 / LVDS_RXp11		120	U11	B19p	3	64.818	R63			JP1C	12
J1	141	D54 / LVDS_TXn11	D54 / LVDS_TXn11		121	Y1	L29n	2	65.302				JP1C	13
J1	142	D55 / LVDS_RXn11	D55 / LVDS_RXn11		122	V11	B19n	3	64.736	R63			JP1C	14
J1	143	+3.3VDD	+3.3VDD		123									
J1	144	+12VDD	+12VDD		124									
J1	145	D56 / LVDS_TXp12	D56 / LVDS_TXp12		125	N7	L30p	2	65.100				JP1C	15
J1	146	D57 / LVDS_RXp12	D57 / LVDS_RXp12		126	AA10	B21p	3	64.473	R64			JP1C	16
J1	147	D58 / LVDS_TXn12	D58 / LVDS_TXn12		127	P7	L30n	2	65.108				JP1C	17
J1	148	D59 / LVDS_RXn12	D59 / LVDS_RXn12		128	AB10	B21n	3	64.389	R64			JP1C	18
J1	149	+3.3VDD	+3.3VDD		129									
J1	150	+12VDD	+12VDD		130									
J1	151	D60 / LVDS_TXp13	D60 / LVDS_TXp13		131	P6	L32p	2	64.200				JP1C	19

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	152	D61 / LVDS_RXp13	D61 / LVDS_RXp13		132	P17	R30p	5	64.393	R65			JP1C	20
J1	153	D62 / LVDS_TXn13	D62 / LVDS_TXn13		133	R5	L32n	2	64.133				JP1C	21
J1	154	D63 / LVDS_RXn13	D63 / LVDS_RXn13		134	R17	R30n	5	64.417	R65			JP1C	22
J1	155	+3.3VDD	+3.3VDD		135									
J1	156	+12VDD	+12VDD		136									
J1	157	D64 / LVDS_TXp14	D64 / LVDS_TXp14		137	U19	R34p	5	64.232				JP1C	23
J1	158	D65 / LVDS_RXp14	D65 / LVDS_RXp14		138	T19	R31p	5	64.935	R66			JP1C	24
J1	159	D66 / LVDS_TXn14	D66 / LVDS_TXn14		139	U20	R34n	5	64.270				JP1C	25
J1	160	D67 / LVDS_RXn14	D67 / LVDS_RXn14		140	T20	R31n	5	64.925	R66			JP1C	26
J1	161	+3.3VDD	+3.3VDD		141									
J1	162	+12VDD	+12VDD		142									
J1	163	D68 / LVDS_TXp15	D68 / LVDS_TXp15		143	Y21	R35p	5	64.614				JP1C	27
J1	164	D69 / LVDS_RXp15	D69 / LVDS_RXp15		144	V21	R29p	5	64.079	R67			JP1C	28
J1	165	D70 / LVDS_TXn15	D70 / LVDS_TXn15		145	Y22	R35n	5	64.672				JP1C	29
J1	166	D71 / LVDS_RXn15	D71 / LVDS_RXn15		146	V22	R29n	5	64.177	R67			JP1C	30

Connector	Pin	HSMC	HSMC+ok	HSMC+ok Jumper Silkscreen	ASP-122953-01	FPGA Pin	FPGA Pin Description	I/O Bank	Length (mm)	LVDS Term RefDes	Comments	EVB 1007	BRK4310 Connector	BRK4310 Pin
J1	167	+3.3VDD	+3.3VDD		147									
J1	168	+12VDD	+12VDD		148									
J1	169	D72 / LVDS_TXp16	D72 / LVDS_TXp16		149	W21	R32p	5	64.355				JP1C	31
J1	170	D73 / LVDS_RXp16	D73 / LVDS_RXp16		150	U21	R27p	5	64.251	R68			JP1C	32
J1	171	D74 / LVDS_TXn16	D74 / LVDS_TXn16		151	W22	R32n	5	64.329				JP1C	33
J1	172	D75 / LVDS_RXn16	D75 / LVDS_RXn16		152	U22	R27n	5	64.237	R68			JP1C	34
J1	173	+3.3VDD	+3.3VDD		153									
J1	174	+12VDD	+12VDD		154									
J1	175	D76 / CLKOUT2p	D76 / CLKOUT2p		155	T5	L33p	2	65.126				JP1C	35
J1	176	D77 / CLKIN2p	D77 / CLKIN2p		156	N5	L22n	2	64.389 / 64.993	R70	See UM for CLKIN jumper selection. Move R112 to R110 for FPGA pin T2 (CLK2, DIFFCLK_1p) in Bank 2.		JP1C	36
J1	177	D78 / CLKOUT2n	D78 / CLKOUT2n		157	R6	L33n	2	65.127				JP1C	37
J1	178	D79 / CLKIN2n	D79 / CLKIN2n		158	P5	L26p	2	64.389 / 64.929	R70	See UM for CLKIN jumper selection. Move R114 to R116 for FPGA pin T1 (CLK3, DIFFCLK_1n) in Bank 2.		JP1C	38
J1	179	+3.3VDD	+3.3VDD		159									
J1	180	PRSNTn	PRSNTn		160						Present Detect			