

# Pin List: XEM6001

2024-11-10

| Connector | Pin | FPGA Pin | Description |
|-----------|-----|----------|-------------|
| JP2       | 1   |          | DGND        |
| JP2       | 2   |          | DGND        |
| JP2       | 3   |          | SYS CLK 5   |
| JP2       | 4   | J4       | I/O / GCLK  |
| JP2       | 5   | A2       | I/O         |
| JP2       | 6   | A3       | I/O         |
| JP2       | 7   | B1       | I/O         |
| JP2       | 8   | B2       | I/O         |
| JP2       | 9   |          | +3.3VDD     |
| JP2       | 10  |          | +3.3VDD     |
| JP2       | 11  | C3       | I/O         |
| JP2       | 12  | C2       | I/O         |
| JP2       | 13  | C1       | I/O         |
| JP2       | 14  | D3       | I/O         |
| JP2       | 15  | D1       | I/O         |
| JP2       | 16  | E3       | I/O         |
| JP2       | 17  | E1       | I/O         |
| JP2       | 18  | E2       | I/O         |
| JP2       | 19  |          | DGND        |
| JP2       | 20  |          | DGND        |
| JP2       | 21  | F3       | I/O         |
| JP2       | 22  | F2       | I/O / GCLK  |
| JP2       | 23  | F1       | I/O / GCLK  |
| JP2       | 24  | G3       | I/O         |
| JP2       | 25  | G1       | I/O         |
| JP2       | 26  | H3       | I/O / GCLK  |
| JP2       | 27  | H2       | I/O         |
| JP2       | 28  | H1       | I/O         |
| JP2       | 29  | K1       | I/O         |
| JP2       | 30  | J1       | I/O         |
| JP2       | 31  |          | DGND        |

| Connector | Pin | FPGA Pin | Description |
|-----------|-----|----------|-------------|
| JP2       | 32  |          | DGND        |
| JP2       | 33  | J3       | I/O         |
| JP2       | 34  | K2       | I/O         |
| JP2       | 35  | K3       | I/O / GCLK  |
| JP2       | 36  | L3       | I/O         |
| JP2       | 37  | M3       | I/O         |
| JP2       | 38  | N3       | I/O         |
| JP2       | 39  | L1       | I/O         |
| JP2       | 40  | M1       | I/O         |
| JP2       | 41  |          | +3.3VDD     |
| JP2       | 42  |          | +3.3VDD     |
| JP2       | 43  | M2       | I/O         |
| JP2       | 44  | N1       | I/O         |
| JP2       | 45  | P1       | I/O         |
| JP2       | 46  | P2       | I/O         |
| JP2       | 47  | R1       | I/O         |
| JP2       | 48  | R2       | I/O         |
| JP2       | 49  |          | DGND        |
| JP2       | 50  |          | DGND        |
| JP3       | 1   |          | DGND        |
| JP3       | 2   |          | DGND        |
| JP3       | 3   | B15      | I/O         |
| JP3       | 4   | B16      | I/O         |
| JP3       | 5   | C15      | I/O         |
| JP3       | 6   | C16      | I/O         |
| JP3       | 7   | D16      | I/O         |
| JP3       | 8   | D14      | I/O         |
| JP3       | 9   |          | +3.3VDD     |
| JP3       | 10  |          | +3.3VDD     |
| JP3       | 11  | E15      | I/O         |
| JP3       | 12  | E16      | I/O         |
| JP3       | 13  | F15      | I/O         |
| JP3       | 14  | F14      | I/O         |
| JP3       | 15  | F16      | I/O         |

| Connector | Pin | FPGA Pin | Description |
|-----------|-----|----------|-------------|
| JP3       | 16  | G16      | I/O         |
| JP3       | 17  | G14      | I/O         |
| JP3       | 18  | H15      | I/O         |
| JP3       | 19  |          | DGND        |
| JP3       | 20  |          | DGND        |
| JP3       | 21  | H14      | I/O         |
| JP3       | 22  | H16      | I/O         |
| JP3       | 23  | J16      | I/O / GCLK  |
| JP3       | 24  | J14      | I/O / GCLK  |
| JP3       | 25  | K15      | I/O         |
| JP3       | 26  | K16      | I/O         |
| JP3       | 27  | K14      | I/O / GCLK  |
| JP3       | 28  | L16      | I/O         |
| JP3       | 29  | L14      | I/O         |
| JP3       | 30  | M16      | I/O         |
| JP3       | 31  |          | DGND        |
| JP3       | 32  |          | DGND        |
| JP3       | 33  | M14      | I/O         |
| JP3       | 34  | M15      | I/O         |
| JP3       | 35  | N14      | I/O         |
| JP3       | 36  | N16      | I/O         |
| JP3       | 37  | P15      | I/O         |
| JP3       | 38  | P16      | I/O         |
| JP3       | 39  | R15      | I/O         |
| JP3       | 40  | R16      | I/O         |
| JP3       | 41  |          | +3.3VDD     |
| JP3       | 42  |          | +3.3VDD     |
| JP3       | 43  | R14      | I/O         |
| JP3       | 44  | T15      | I/O         |
| JP3       | 45  | T13      | I/O         |
| JP3       | 46  | T14      | I/O         |
| JP3       | 47  | J13      | I/O / GCLK  |
| JP3       | 48  |          | SYS CLK 4   |
| JP3       | 49  |          | DGND        |

| Connector | Pin | FPGA Pin | Description |
|-----------|-----|----------|-------------|
| JP3       | 50  |          | DGND        |
| JP1       | 1   |          | +3.3VDD     |
| JP1       | 2   |          | +3.3VDD     |
| JP1       | 3   | C7       | I/O         |
| JP1       | 4   | C8       | I/O         |
| JP1       | 5   | A8       | I/O         |
| JP1       | 6   | B8       | I/O         |
| JP1       | 7   | A9       | I/O / GCLK  |
| JP1       | 8   | C9       | I/O / GCLK  |
| JP1       | 9   | A11      | I/O         |
| JP1       | 10  | C11      | I/O         |
| JP1       | 11  | A12      | I/O         |
| JP1       | 12  | B12      | I/O         |
| JP1       | 13  | A13      | I/O         |
| JP1       | 14  | A14      | I/O         |
| JP1       | 15  | B14      | I/O         |
| JP1       | 16  | C13      | I/O         |
| JP1       | 17  | B10      | I/O / GCLK  |
| JP1       | 18  | A10      | I/O / GCLK  |
| JP1       | 19  |          | DGND        |
| JP1       | 20  |          | DGND        |