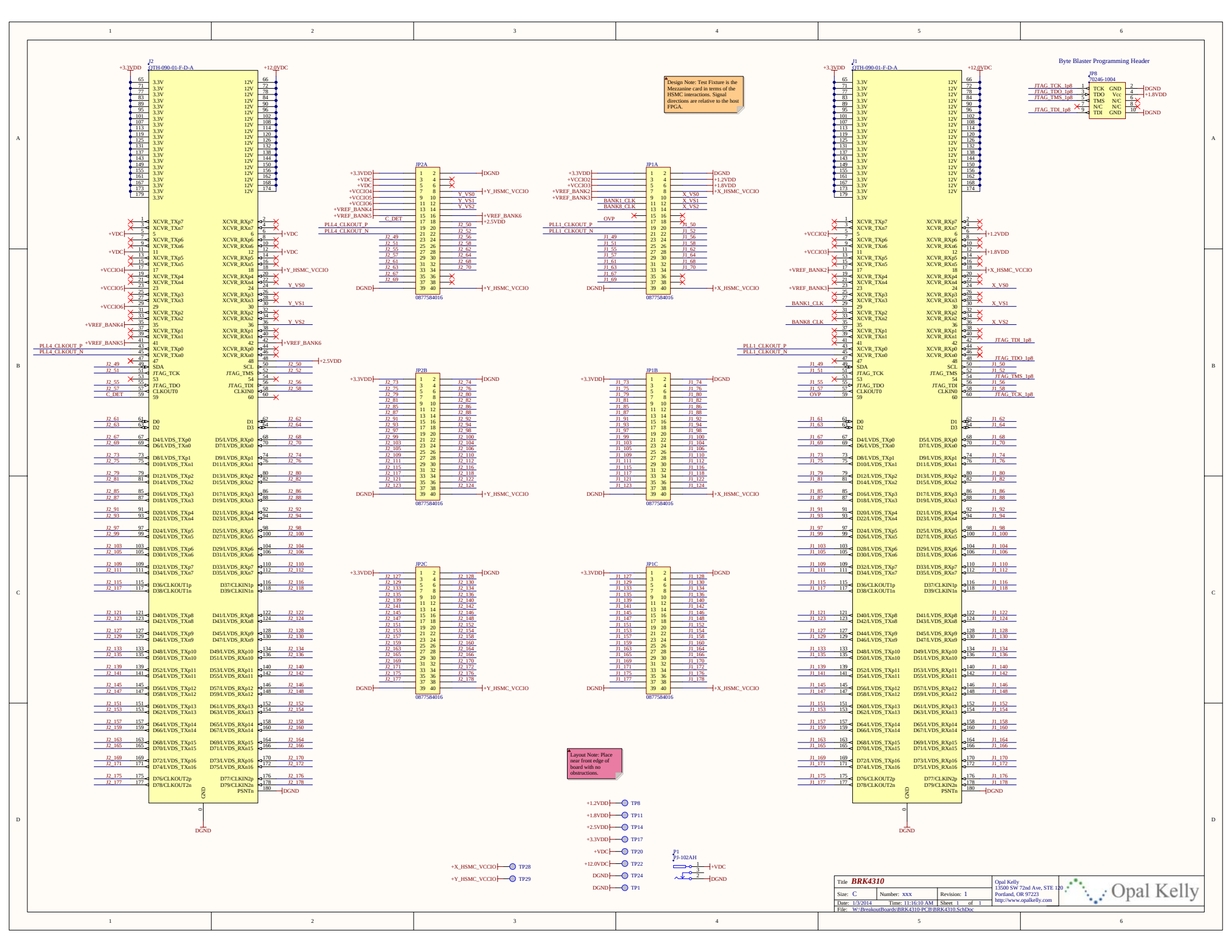
J2
QTH-090-01-F-D-A
J1
QTH-090-01-F-D-A
Byte Blaster Programming Header
JP8
70246-1004
Design Note: Test Fixture is the Mezzanine card in terms of the HSMC interactions. Signal directions are relative to the host FPGA.
JP2A
JP2B
JP2C
JP1A
JP1B
JP1C
0877584016
Layout Note: Place near front edge of board with no obstructions.
J3
PJ-102AH
Title BRK4310
Size: C
Number: xxx
Revision: 1
Date: 1/3/2014
Time: 11:16:10 AM
Sheet 1 of 1
File: W:\BreakoutBoards\BRK4310-PCB\BRK4310.SchDoc
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